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Abstract
As CMOS devices have been scaled down, the channel length shrinks and the absolute value of threshold voltage becomes smaller due to the reduced controllability of the gate over depletion region by the increased charge-sharing from the source/drain. Therefore, the study of short-channel effects (SCEs) have assumed a significant role because both the threshold voltage roll-off at decreasing gate length as well as drain-induced barrier lowering (DIBL) at increasing drain voltage pose a serious challenge to the efforts for down-scaling the CMOS technology. Double-Gate (DG) MOSFETs seem to be a very promising option for ultimate scaling of CMOS technology. In this dissertation, a physical and analytical model is developed for short-channel effects (SCEs) in fully depleted double-gate (DG) MOSFETs. On the base of resultant solution for 2-D Poisson's equation included in both silicon film and gate oxide regions, the physical and analytical model including threshold voltage, subthreshold swing, and 2-D electrostatic potential for the short-channel fully depleted symmetrical double-gate (SDG) MOSFETs is developed. These analytical results can be used to model of DG MOSFET's. The results calculated by the model agree well with the simulation data without any fitting parameters. They are also extendable to high-k gate insulators for precisely predicting the fringing field effects with high-k gate dielectrics.
To enhance the immunity against SCEs, a new structure called the dual-material gate (DMG) MOSFET has been proposed. In the DMG MOSFET, the work function of metal gate 1 (M1) is greater than metal gate 2 (M2) i.e., $>$ and hence, threshold voltage $>$ which has the inherent advantage of improving the gate transport efficiency by modifying the electric field pattern and the surface potential along the channel. Based on fully resultant 2-D potential solution, the physical and precisely analytical model for the short-channel fully depleted symmetrical dual-material double-gate (SDMDG) MOSFETs is successfully developed. The simulated results of the analytical model match well with those simulated by device simulator. Besides giving deep insight into the device physics,

the analytical results are useful in compact modeling the threshold voltage of short-channel SDMDG MOSFET.
As the channel lengths of MOSFETs push into the nanometer regime, short-channel effects (SCEs) become intensively significant and put a hard limit to MOSFET performance. The design of optimal DG devices will require new insights into the underlying physics, especially the quantum mechanics (QM) of the carriers confined in very thin (tsi $\leqq$ 10 nm) Si films. Quantum-mechanical confinement of inversion-layer carriers significantly affects the threshold voltage and gate capacitance of highly scaled MOSFETs. In this dissertation, we present a physical threshold voltage model in subthreshold region, and use analytical solutions to give design insight regarding the quantum effects in symmetrical DG MOSFETs. Quantization effects on DG MOSFET scalability is also examined in the thesis. This thesis not only provides a simple and computation-efficient short-channel surface potential and threshold voltage analytical model, but also offers the basic designing guideline for fully-depleted DG MOSFET.
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